modulation (PCM) signal having n bits and then outputting a pulse width modulation (PWM) signal. The MPWM DAC comprises a converter circuit, a control device, a first output driver device, a second output driver device and an output device.

The converter circuit converts (n-m) bits of the PCM signal into the PWM signal, wherein m is the number of the least significant bit (LSB) signal of the PCM signal and n>m. Each of the first output driver device and the second output driver has different number of output drivers, thereby the output PWM signal is a multi-level signal, rather that a two-level signal in the prior art.

In The Claims

Please amend independent claims 1 and 8 as follows

1. (Once Amended) A multi-level pulse width modulation (MPWM) digital-to-analog converter for receiving a pulse code modulation (PCM) signal having n bits and then outputting a pulse width modulation (PWM) signal , comprising:

a converter circuit for receiving the PCM signal to convert (n-m) bits of the PCM signal into the PWM signal, wherein m is the number of the least significant bit (LSB) signal of the PCM signal and n>m, and then generating a first input signal, a second input signal and an enabling signal;

a control device for receiving the enabling signal to generate a control signal;

a first output driver device having 2^{m1} output drivers (m1<n) for receiving the first input signal and the control signal, and then outputting a first driving signal, wherein sum of output currents of the 2^{m1} output drivers is equal to a maximum output current of the first output driver device;

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a second output driver device having 2^{m2} output drivers (m2<n) for receiving the second input signal and the control signal, and then outputting a second driving signal, wherein sum of output currents of the 2^{m2} output drivers is equal to a maximum output current of the second output driver device; and

an output device for receiving the first and the second driving signals and then outputting the PWM signal;

wherein in response to the least significant bit (LSB) signal of the PCM signal, the control device selects and disables in a specified interval of each sampling cycle such that the output drivers the first and the second output driver devices are in a high impedance status, to control outputs of the first and the second output driver devices.

8. (Once Amended) A multi-level pulse width modulation (MPWM) digital-to-analog converter for receiving a digital signal, wherein the digital signal comprises at least one modulated bit and at least one level bit and then outputs an analog modulated signal, comprising:

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a converter circuit for receiving the digital signal and then converting the modulated bit into a first output signal, a second output signal, and the converter circuit outputting the first output signal, the second output signal and the level bit of the digital signal;

a control device for receiving the level bit of the digital signal to generate a control signal;

a plurality of first output drivers for receiving the first input signal and the control signal, and then outputting a first driving signal, wherein sum of output currents of the first output drivers is equal to a maximum output current corresponding to the first driving signal;

a plurality of second output drivers for receiving the second input signal and the control signal, and then outputting a second driving signal, wherein sum of output currents of the first output drivers is equal to a maximum output current corresponding to the first driving signal; and

an output device for receiving the first and the second driving signals and then outputting the analog modulated signal.